IN THE CLAIMS:

Please cancel claims 8-10 without prejudice or disclaimer, and amend claims 13-15 as follows:

1. (Original) A phase shifter for shifting a phase relation between a clock signal and a data signal, the phase shifter comprising:

a first filter that inputs at least one of the clock signal and the data signal to be phase-shifted;

a first signal path and a second signal path that divide an output signal from the first filter to input divided signals;

a phase shift element that gives different phases to one of the divided signals on the first signal path and another of the divided signals on the second signal path;

a first variable gain amplifier located on the first signal path;

a second variable gain amplifier located on the second signal path;

an adder-subtractor that executes an operation to an output from the first variable gain amplifier and an output from the second variable gain amplifier;

a second filter that inputs an output from the adder-subtractor; and

control means that adjusts at least one output of the first and second variable gain amplifiers to thereby adjust the phase of the output from the second filter.

2. (Original) The phase shifter according to claim 1, wherein the first filter is a low-pass filter that passes low frequency factors of an input signal.

3. (Original) The phase shifter according to claim 2, wherein the first filter is the low pass filter that eliminates higher-order frequency factors of the input signal than the frequency of a base clock signal.

4. (Original) The phase shifter according to claim 1, wherein the phase shifter element is a 90-degree phase shifter that gives the a 90° phase shift to an input signal.

5. (Original) The phase shifter according to claim 1, wherein the adder-subtractor executes addition or subtraction to input signals.

6. (Original) The phase shifter according to claim 1, wherein the second filter is a limit amplifier that converts a signal having a low frequency factor of an input signal or a signal having a frequency equal to the frequency of a base clock signal into a rectangular wave signal.

7. (Original) The phase shifter according to claim 1, wherein all the circuits are comprised of analog circuits.

8-10. (Cancelled)

11. (Original) A skew compensation system used for high-speed parallel signaling, wherein the skew compensation system shifts phase differences between a high-speed synchronized clock signal and parallel data signals, the skew compensation system comprising:

a phase shifting circuit located on a receiver side for controlling phase differences between the clock signal and the parallel data signals; wherein a special data pattern defined to be used is transmitted when a synchronized data transmission cannot be realized because of a skew between parallel data lines being not yet adjusted on the receiver side or before transmitting the data signals every constant time cycle from a transmitter side; and wherein the phase shifting circuit receives signals outputted from a transmitter side circuit to detect errors of the signals to the defined special data pattern, and compensates the skew between the clock signal and the data signals on basis of a result of the detection at the receiver side so that a phase relation for receiving the special data pattern correctly at the receiver side is obtained, and

a circuit that the phase shifting circuit has,

wherein the circuit, in order to shifts the phase of either of the clock signal or the parallel data signals by dividing the phase for one cycle of the base frequency of the synchronized clock signal into time cycles of x units (x: integer not less than 2) with even time cycle or uneven time cycle to compensate the skew, executes a filtering processing to one of the clock signal or the data signals through a band pass filter having a pass band not higher than the base frequency of the synchronized clock signal, divides the filtered signal into plural signals of more than or equal to two, inputs the signals after being divided to phase shifter elements each having different

propagation delay characteristics, inputs signals from the phase shifter elements to different variable gain amplifiers respectively, after adding outputs from the variable gain amplifiers, inputs a signal after being added to a limit amplifier having a pass band characteristic sufficiently higher than the based frequency of the synchronized clock signal to reshape the waveform of the signal after being added into a rectangular wave, and inputs a signal after being reshaped to a flip-flop circuit together with the parallel data signals or the clock signal paired with the reshaped signal to execute a re-timing processing, and

wherein the phase shifting circuit, by individually adjusting the outputs from the plural variable gain amplifiers incorporated in the circuit, shifts the phases of the output signals from the limit amplifier of the data signals or the clock signal to be phase-shifted to x levels with the signal factors retained intact, and realizes shifting the phase differences between the clock signal and the data signals by using the above phase-shifting function.

12. (Original) A skew compensation system used for high-speed parallel signaling, wherein the skew compensation system shifts phase differences between a high-speed synchronized clock signal and parallel data signals, the skew compensation system comprising:

a first circuit located on a receiver side for controlling phase differences between the clock signal and the parallel data signals; wherein a special data pattern defined to be used is transmitted when a synchronized data transmission cannot be realized because of a skew between parallel data lines being not yet adjusted on the receiver side or before transmitting the data signals every constant time cycle from a transmitter side; and wherein the first circuit receives signals outputted from a transmitter side circuit to detect errors of the signals to the defined special data pattern, and adjusts the phase differences between the clock signal and the data signals on basis of a result of the detection at the receiver side of the data so that a phase relation for receiving the special data pattern correctly at the receiver side is obtained, and

a second circuit that the first circuit has,

wherein the second circuit, in order to shifts the phase of either of the clock signal or the data signals by dividing the phase for one cycle of the base frequency of the synchronized clock signal into time cycles of x units (x: integer not less than 2)

with even time cycle or uneven time cycle, executes a filtering processing to one of the clock signal or the data signals through a band pass filter having a pass band not higher than the base frequency of the synchronized clock signal, divides the filtered signal into plural signals of more than or equal to two, inputs the signals after being divided to phase shifter elements each having different propagation delay characteristics, inputs signals from the phase shifter elements to different variable gain amplifiers respectively, after adding or subtracting outputs from the variable gain amplifiers by means of an adder-subtracter, inputs a signal after being added or subtracted to a limit amplifier to a limit amplifier having a pass band characteristic sufficiently higher than the based frequency of the synchronized clock signal to reshape the waveform of the signal after being added or subtracted into a rectangular wave, and inputs a signal after being reshaped to a flip-flop circuit together with the data signals or the clock signal paired with the reshaped signal to execute a re-timing processing, and

wherein the first circuit, by individually adjusting the outputs from the plural variable gain amplifiers incorporated in the second circuit and using to switch the adding and subtracting functions, shifts the phases of the output signals from the limit amplifier of the data signals or the clock signal to be phase-shifted to x levels with the signal factors retained intact, and realizes shifting the phase differences between the clock signal and the data signals by using the above phase-shifting function.

13. (Currently Amended) The skew compensation system according to claim [[10]]11, further comprising a circuit capable of variable adjustment as to either or both of the dividing number x of the phase shifting and the time cycle of the phase shifting.

14. (Currently Amended) The skew compensation system according to claim [[10]]11, further comprising a circuit capable of variable adjustment as to the propagation delay characteristics of all or part of the phase shifter elements located on the pre-stage of the variable gain amplifiers inside the skew compensation system.

15. (Currently Amended) The skew compensation system according to claim [[10]]11, wherein a combination of special characters of 8B10B code or 64B66B code used in the Ethernet (trademark) standard is used as the special data pattern for the skew compensation.

16. (Previously Presented) The skew compensation system according to claim 11, further comprising a circuit capable of variable adjustment as to either or both of the dividing number x of the phase shifting and the time cycle of the phase shifting.

17. (Previously Presented) The skew compensation system according to claim 12, further comprising a circuit capable of variable adjustment as to either or both of the dividing number x of the phase shifting and the time cycle of the phase shifting.

18 (Previously Presented) The skew compensation system according to claim 12, further comprising a circuit capable of variable adjustment as to the propagation delay characteristics of all or part of the phase shifter elements located on the pre-stage of the variable gain amplifiers inside the skew compensation system.

19. (Previously Presented) A skew compensation system according to claim 11, wherein a combination of special characters of 8B10B code or 64B66B code used in the Ethernet (trademark) standard is used as the special data pattern for the skew compensation.

20. (Previously Presented) A skew compensation system according to claim 12, wherein a combination of special characters of 8B10B code or 64B66B code used in the Ethernet (trademark) standard is used as the special data pattern for the skew compensation.